In the Claims:

Claim 41 (amended). The apparatus according to claim 40, wherein:

a signal bus is connected to said initial state registers, said at least one transition register, and said final state registers;

said at least one multiplexer includes:

a first multiplexer having:

a control input;

a first data input; and

a second data input;

a second multiplexer having:

a control input;

a first data input; and

a second data input;

a third multiplexer having:

a control input;

a first data input; and

a second data input;

said evaluation units include:

a trace-back register with a first data output, a first data input, and a second data output;

comparison units; and

maximum selection elements including a first maximum selection element with an output;

said selection register has an input connected to said signal bus and an output connected to said control input of said first multiplexer;

said first data input of said first multiplexer is connected to said first data output of said trace-back register;

said second data input of said first multiplexer is connected to said output of said first maximum selection element;

said control input of said second multiplexer is connected to said first data input of said trace-back register;

said first data input of said second multiplexer is connected to said output of said second adder;

said second data input of said second multiplexer is connected to said output of said third subtracter;

said comparison units include:

a first comparator; and

a second comparator with a second comparator output

said control input of said third multiplexer is connected to said second comparator output;

said first data input of said third multiplexer is connected to said output of said second subtracter; and

said second data input of said third multiplexer is connected to said output of said third adder.